National Semiconductor

MICROCIRCUIT DATA SHEET

MNLM137-WG REV 0A0

Original Creation Date: 03/04/02
Last Update Date: 03/15/02
Last Major Revision Date:

3-TERMINAL VOLTAGE REGULATOR, -37 VOLTS ≤ VO ≤ -1.25 VOLTS AT 0.5A

General Description

The LM137H is an adjustable 3-terminal negative voltage regulator capable of supplying in excess of -0.5A over an output voltage range of -1.2V to -37V. This regulator is exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Futher, the LM137H features internal current limiting, thermal shutdown and safe-area compensation, making it virtually blowout-proof against overloads.

The LM137H serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137H is an ideal complement to the LM117H adjustable positive regulator.

Industry Part Number

LM137

NS Part Numbers

LM137WG-QMLV

Prime Die

LM137

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Output voltage adjustable from -1.2V to -37V
- 0.5A output current guaranteed, -55 C to +150 C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 50 ppm/ C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- Stantard 3-lead transistor package
- Output short circuit protected
- CONTROLLING DOCUMENTS:
  LM137WG-QMLV 5962-9951701VZA

(Absolute Maximum Ratings)

(Note 1)

Power Dissipation	Internally Limited
Input-Output Voltage Differential	40V
Operatuing Junction Temperature	-55 C ≤ Ta ≤ +150 C
Maximum Junction Temperature (Note 2)	150 C
Maximum Power Dissipation (@ 25 C)	2.5 Watts
Minimum Input Voltage	-41.25V
Storage Temperature	-65 C ≤ Ta ≤ +150 C
Lead Temperature (Soldering, 10 seconds)	300 C
Thermal Resistance	
ThetaJA	
CERAMIC SOIC	
(Still Air @ 0.5W)	108 C/W
(500LF/Min Air Flow @ 0.5W)	65 C/W
ThetaJC	
CERAMIC SOIC (@ 1.0W)	2.7 C/W
Package Weight (Typical)	
CERAMIC SOIC	370mg
ESD Rating (Note 3)	4000V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA) /ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: For the CERAMIC SOIC device to function properly, the "Output" and "Output/Sense" pins must be connected on the users printed circuit board.

Note 4: The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using junction-to-ambient, rather than junction -to-case, thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out the package, since the thermal resistance of the leadframe material is very poor, relative to the material of the package base. The stated junction-to-case thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.

Note 5: Human body model, 1.5K Ohms in series with 100pF.

Recommended Operating Conditions

Ta	-55 C ≤ Ta ≤ +125 C
Input Voltage Range	-41.25V to -4.25V

Electrical Characteristics

DC PARAMETERS:

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vout	Output Voltage	Vin = -4.25V, Il = 5mA			-1.275	-1.225	V	1
					-1.3	-1.2	V	2, 3
		Vin = -4.25V, Il = 500mA			-1.275	-1.225	V	1
					-1.3	-1.2	V	2, 3
		Vin = -41.25V, Il = 5mA			-1.275	-1.225	V	1
					-1.3	-1.2	V	2, 3
		Vin = -41.25V, Il = 50mA			-1.275	-1.225	V	1
					-1.3	-1.2	V	2, 3
Vrline	Line Regulation	Vin = -41.25V to -4.25V, Il = 5mA			-9	9	mV	1
					-23	23	mV	2, 3
Vrload	Load Regulation	Vin = -6.25V, Il = 5mA to 500mA			-12	12	mV	1
					-24	24	mV	2, 3
		Vin = -41.25V, Il = 5mA to 50mA			-6	6	mV	1
					-12	12	mV	2, 3
		Vin = -6.25V, Il = 5mA to 200mA			-6	6	mV	1
					-12	12	mV	2, 3
Vrth	Thermal Regulation	Vin = -14.6V, Il = 500mA			-5	5	mV	1
Iadj	Adjust Pin Current	Vin = -4.25V, Il = 5mA			25	100	uA	1, 2, 3
		Vin = -41.25V, Il = 5mA			25	100	uA	1, 2, 3
Delta Iadj(line)	Adjust Pin Current Change vs. Line Voltage	Vin = -41.25V to -4.25V, Il = 5mA			-5	5	uA	1, 2, 3
Delta Iadj(load)	Adjust Pin Current Change vs. Load Current	Vin = -6.25V, Il = 5mA to 500mA			-5	5	uA	1, 2, 3
Ios	Output Short Circuit Current	Vin = -4.25V			0.5	1.8	A	1, 2, 3
		Vin = -40V			0.05	0.5	A	1, 2, 3
Vout (Recovery)	Output Voltage Recovery After Output Short Circuit Current	Vin = -4.25V			-1.275	-1.225	V	1
					-1.3	-1.2	V	2, 3
		Vin = -40V			-1.275	-1.225	V	1
					-1.3	-1.2	V	2, 3

Electrical Characteristics

DC PARAMETERS:(Continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Iq	Minimum Load Current	Vin = -4.25V			0.2	3	mA	1, 2, 3
		Vin = -14.25V			0.2	3	mA	1, 2, 3
		Vin = -41.25V			1	5	mA	1, 2, 3
Vstart	Voltage Start-up	Vin = -4.25V, Il = 500mA			-1.275	-1.225	V	1
					-1.3	-1.2	V	2, 3
Vout	Output Voltage	Vin = -6.25V, Il = 5mA	1		-1.3	-1.2	V	2

AC PARAMETERS:

Delta Vin/Delta Vout	Ripple Rejection	Vin = -6.25V, Il = 125mA, ei = 1Vrms at 2400Hz			48		dB	9
Vno	Output Noise Voltage	Vin = -6.25V, Il = 50mA				120	uVrms	9
Delta Vout/Delta Vin	Line Transient Response	Vin = -6.25V, Vpulse = -1V, Il = 50mA				80	mV/V	9
Delta Vout/Delta Il	Load Transient Response	Vin = -6.25V, Il = 50mA, Delta Il = 200mA	2			60	mV	9

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: "Delta calculations performed on JAN S and QMLV devices at group B, subgroup 5 only".

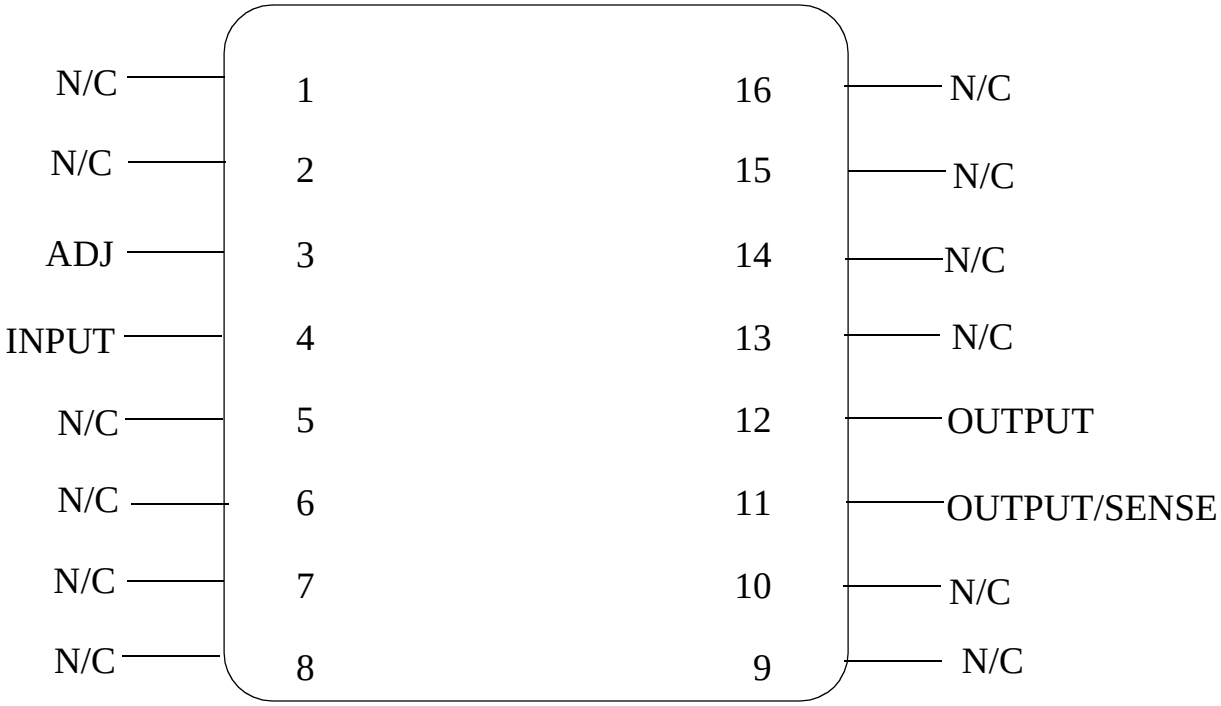
Vout	Output Voltage	Vin = -4.25V, Il = 5mA			-0.01	0.01	V	1
		Vin = -4.25V, Il = 500mA			-0.01	0.01	V	1
		Vin = -41.25V, Il = 5mA			-0.01	0.01	V	1
		Vin = -41.25V, Il = 50mA			-0.01	0.01	V	1
Vrline	Line Regulation	Vin = 41.25V to -4.25V, Il = 5mA			-4	4	mV	1
Iadj	Adjust Pin Current	Vin = -4.25V, Il = 5mA			-10	10	uA	1
		Vin = -41.25V, Il = 5mA			-10	10	uA	1

Note 1: Tested at +125 C; correlated to 150 C.
Note 2: Limit of 0.3mV/mA is equivalent to 60mV.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
06367HRA1	CERAMIC SOIC (WG), 16 LEAD (B/I CKT)
P000463A	CERAMIC SOIC (WG), 16 LEAD (PINOUT)
WG16ARC	CERAMIC SOIC (WG), 16 LEAD (P/P DWG)

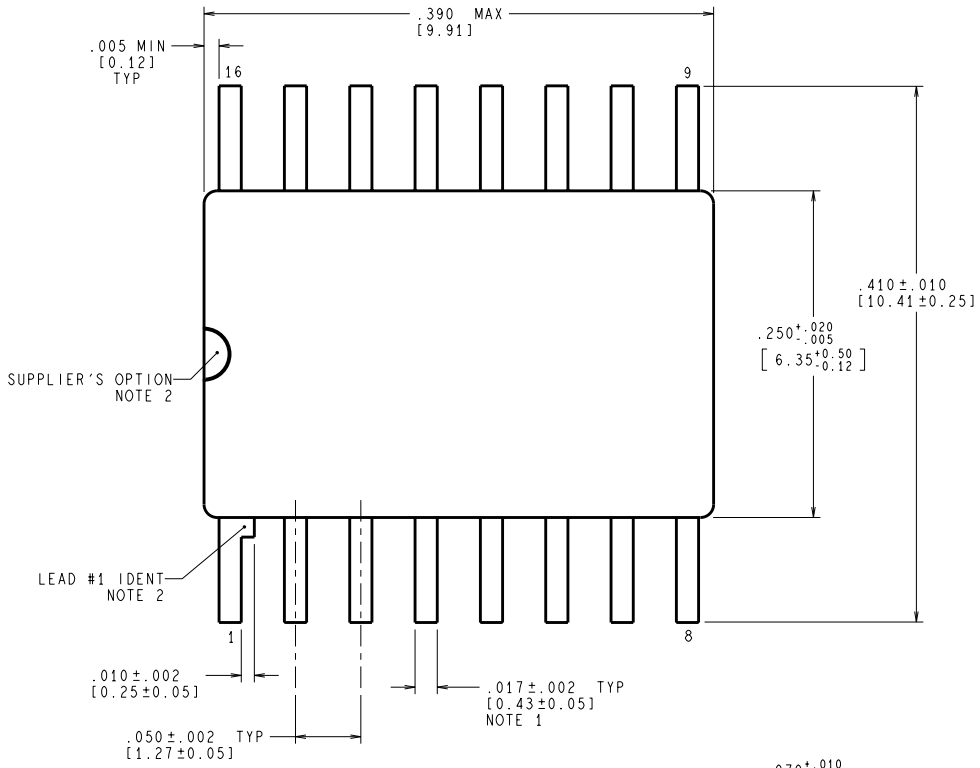
See attached graphics following this page.

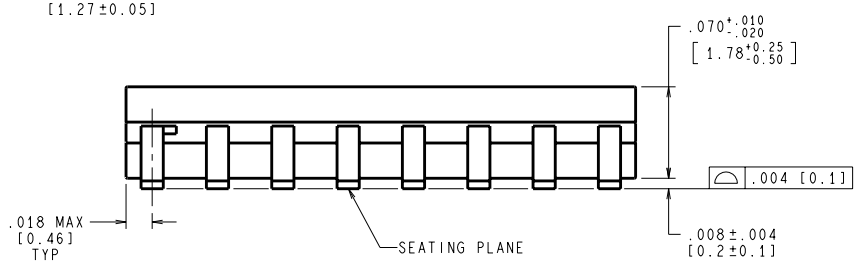


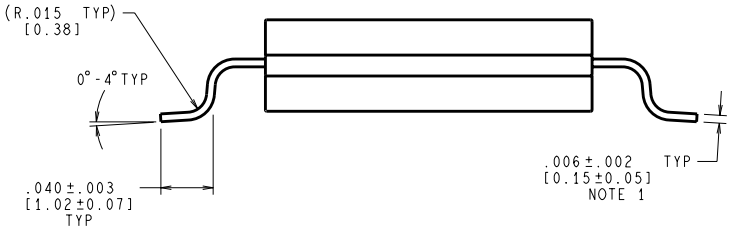
LM137WG
16 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM
TOP VIEW
P000463A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11376	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM .040±.003 WAS .037±.003	11443	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11840	10/08/1997	TL/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

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CERPACK, 16 LEAD, GULL WING

PROJECTION — INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG16A	C

DO NOT SCALE DRAWING — SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0A0	M0003963	03/15/02	Rose Malone	Initial MDS Release: MNLM137-WG, Rev. 0A0.